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Low Power Design of D Flip Flop on CMOS 90nm Technology

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Abstract- In this paper, a D flip flop is designed for efficient power using CMOS 90 nm Technology. The three types designs are proposed as fully automatic, semi-custom and full custom. In fully automatic design, inbuilt active devices are used with auto routing and placement approach. On semicustom design, inbuilt active devices are used along with optimal routing and placement In fully custom design, manual active devices are built along with manual routing and placement. In fully automatic approach proposed schematic is designed in with DSCH and equivalent design is created using Microwind software. In case of semicustom design, optimized layout is created with Microwind. In fully custom design own active devices and manual routing is used to generate optimized layout. It is observed from simulated results that power is improved by 26 % and area is improved by 52% in case of fully custom design compared with fully automatic design. The semicustom design power is slightly increased compared with fully automatic design.

Index Terms- Flip-Flop , Pulse triggered, low Powered, PDP

1. INTRODUCTION

Flip Flop is a memory device that can be used to store one bit of information. The D latch 'latches' the logic level on the input line when CLK is high. If data on input line changes the state while the clock is high, then Q, follows, input. When the CLK = 0, the last state of the input is latched [1] .The performance parameter are power consumption (P), propagation delay (Td), power-delay product (PDP) and area of layout. The formula for power consumption is given by following equation

$$P_d = \alpha\, C_L VDD^2 f_{clk} + VDD\, I_{sc} + VDD(\, I_{leakage} + I_{static})$$

Where α = switching factor, Pd = power dissipated, Vdd is connected supply voltage, fclk is frequency of clock signal, CL the load capacitance, Isc is short circuit current, Istatic is direct current from the VCC to GND, and Ileakage = reverse diode leakage current and sub-threshold current . The sum of static power, short circuit power and dynamic power is equal to total power consumption. Static power dissipation occurs when input at LOW, the N-MOS transistor is OFF condition and P-MOS transistor is ON condition. The output is connected to supply voltage VCC, and if the input is at HIGH, the N-MOS transistor is ON and the P-MOS transistor is in OFF condition i.e open circuited condition. The output is connected to GND (logic 0). Important to notice that one of the transistors is always ON and other is OFF when the gate is in one of the logic states. When gate current is zero then there is no path from VCC to GND, therefore steady-state current and static power consumption becomes zero. Dynamic power consumption occurs because of switching between sates. It is sum of the current required to for switching plus the current that flows from VCC to GND .Time delay is calculated between the 50 percent of both input transition and output transition. The delay formula is given as follows:

$$\boldsymbol{T_d = (4C_L V_{DD}\,)/[\,A(V_{DD} - Vt)^2]}$$

Where ,CL is load capacitance, A is constant.,Vdd is supply voltage, Vt is threshold voltage. The trade-off between propagation delay (Td) and VCC always remain in circuit. The power–delay product PDP is a measure for energy efficiency of a logic device or logic family known as switching energy. It is given by following formula. The unit is joules.[1]

PDP= POWER×DELAY (JOULES)

2. SCHEMATIC DESIGN

The NAND based D latch is implemented as shown in figure 1. Clock signal is active low, means the input at D is latched to output Q if CLK=0, otherwise it will remain in last state. The output Q is held as it is when CLK=1. The schematic design is generated in DSCH and Verilog file is generated. 4 NAND gates are used to construct D flip flop,

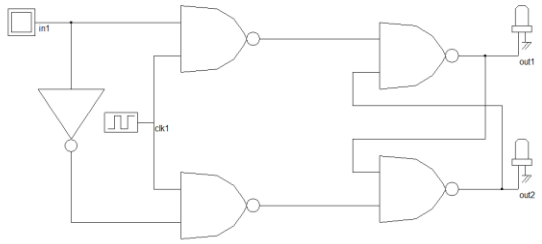


Fig.1. Gate-level schematic of the clocked NAND-based D Flip flop circuit, with active low inputs.

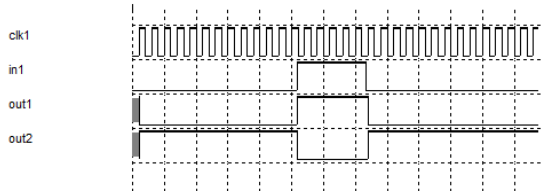


Fig. 2 Waveform of clocked D flip flop

The D flip-flop truth table is shown in Table 1.

Table 1

CLK	D	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
1	0	0	1
0	1	0	1
1	1	1	0

3. LAYOUT DESIGN AND SIMULATION

In first method the schematic of D flip-flop is designed. Using Microwind software the auto generated layout of D flip-flop is created, and then simulates the layout. In this paper 90nm foundry is selected. The figure 3 represents this auto generated layout. This layout is checked for DRC if there is no error then it is simulated. And generated timing waveforms are verified on comparing to the circuit operation. The Power is measured by the simulation result. The figure 4 shows the timing diagram of this automatic layout. We measure the power consuming by this layout and from the properties of layout area is measured. Here the consuming power is 21.65 µWatt. Area required for this particular layout is 57.42µm2 .Width is 7.8 µm and height is 7.4 µm.

In second step we prepare layout using semicustom approach. In semicustom approach transistors are in-built. In this approach connections are made by the developer following lambda design rules. There is possibility of power reduction. Figure 5 represents the layout using semicustom approach

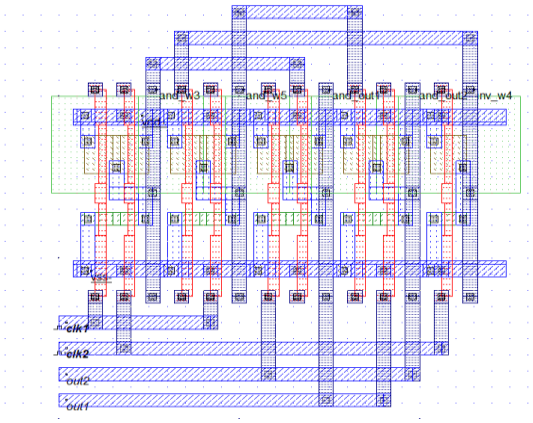


Fig. 3 Fully Automatic D flip-flop

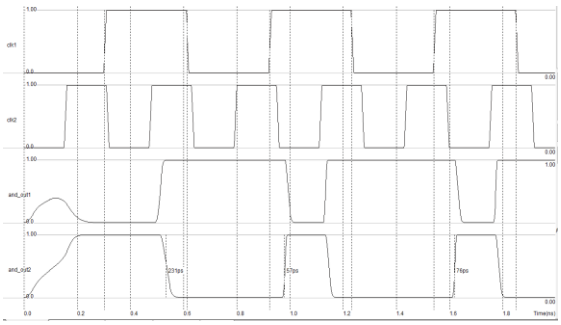


Fig.4. Timing Diagram of Fully Automatic Layout

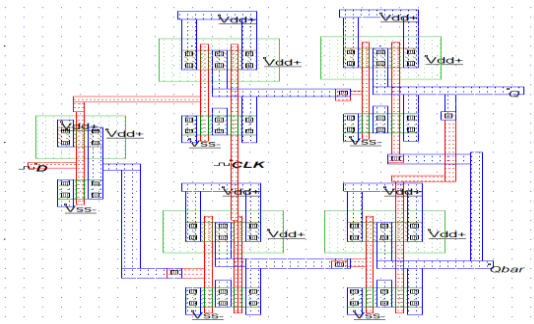


Fig. 5. Semi-custom Layout of D flip-flop

The semicustom layout is checked for DRC if there is no error present in layout, the circuit is simulated and timing waveforms are generated. The generated timing waveforms are verified with the truth table or operation of original circuit. Figure 6 shows the timing diagram of semicustom layout.

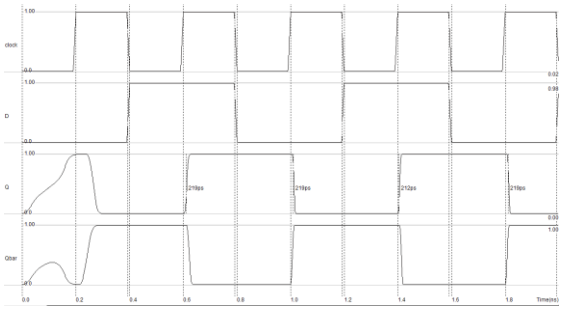


Fig.6. Timing Diagram of Semi-custom layout

The power is observed from this particular simulation. Here power is 22.98 µWatt, slightly more than automatic layout and area is calculated from the properties. Here the width is 7.0 µm and height is 7.9 µm . In semicustom layout area is 55.3 µm2. In fully custom design a transistor is designed and checked for DRC if there is no error, the circuit of D flip flop is generated using this nMOS and pMOS transistor. The generated waveforms are verified with truth able and operation of original circuit. Figure 7 shows the layout for fully custom design.

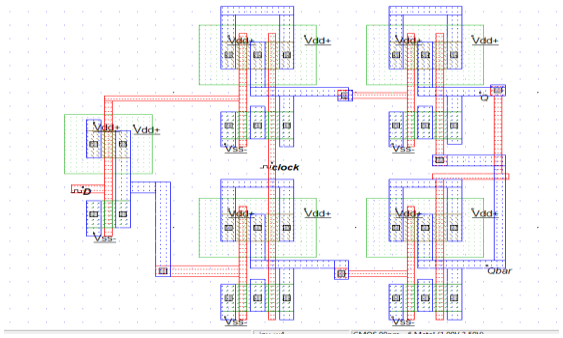


Figure 7 Fully custom design of D flip flop.

Here power is 15.924 µWatt, which is significantly less than auto generated and semi-custom design. Here the area is also significantly less than rest two design methods. Here width is 5.6 µm and height is 4.9 µm. In fully custom layout is 27.44 µm2. Figure 8 shows the timing diagram of fully custom design.

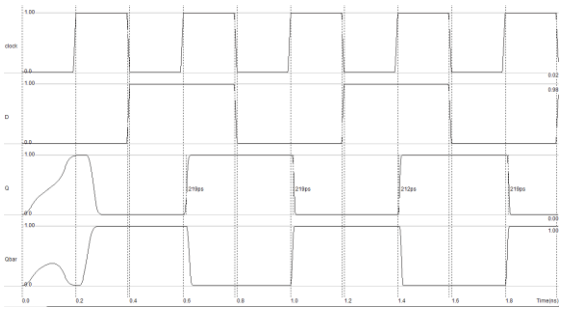


Figure 8 Timing Diagram of Fully custom layouts

4. RESULTS

The performance of proposed D flip flop fully custom layout is compared with semicustom and auto generated approach layout. The performance parameters are area and Power. From above results a comparative study can be done between three designing approaches. Table 2 shows comparative analysis.

Table 2: Comparison for Area and Power

Design	Fully Auto	Semicustom	Fully custom
Area(µm2)	57.72	55.3	27.44
Power(µWatt)	21.65	22.98	15.92

Table 3: Bar graph for Area

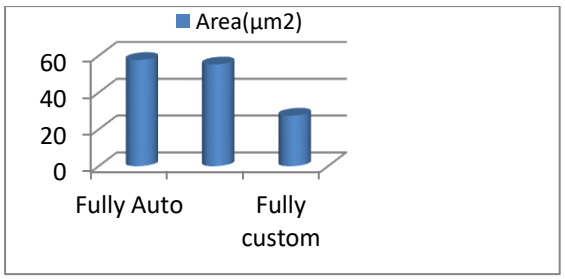
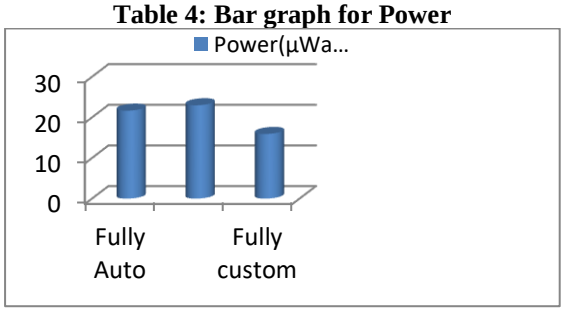


Table 4: Bar graph for Power



5. CONCLUSION

The results show that the fully custom design is optimized in terms of area and power. Fully automated design shows power of 21.65 µwatt and area of 57.72 µm2. There is significant reduction in power to 15.92 µWatt and area to 27.44 µm2 in fully custom design compared to fully automatic design. In Semi-custom design is slightly reduction in area but the power is slightly increased compared with fully automatic design. This fully

custom design can be used in circuits where the power and area are main constraint of design.

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